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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,228	04/16/2004	Gregory Hogdal	MSI-671USC1	9654
22801	7590	01/19/2006	EXAMINER	
LEE & HAYES PLLC 421 W RIVERSIDE AVENUE SUITE 500 SPOKANE, WA 99201			MCCARTHY, CHRISTOPHER S	
			ART UNIT	PAPER NUMBER
			2113	
DATE MAILED: 01/19/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/826,228	HOGDAL ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 16 April 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 15-25 is/are rejected.
- 7) ☒ Claim(s) 14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>4/16/04</u> .   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 5 is objected to because of the following informalities: there is no period at the end of the claim. Appropriate correction is required.

### ***Double Patenting***

2. Claims 1-25 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5, 8-12, 16-23, 25-30 of U.S. Patent No. 6,766,472. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is well settled that the omission of an element and its function is an obvious expedient if elements perform the same function (In re Karlson, 136 USPQ 184 CCPA 1973).

Claim 1 omits the following element from patented claim 1: whereby a caching scheme is utilized that assumes that a root of memory tables contained in the physical memory data is fixed and does not change after it is initialized.

Claims 2-5 are disclosed as patented claims 2-5, respectively.

Claims 6-10 are disclosed as patented claims 8-12, respectively.

Claims 11 and 19 are disclosed as patented claim 16.

Claims 12-18 are disclosed as patented claims 17-23, respectively.

Claim 20 is disclosed as patented claim 25.

Art Unit: 2113

Claim 21 omits the following element from patented claim 26: debugging a fault that occurred on the target computer by processing the transferred physical memory contents at the host.

Claims 22-25 are disclosed as patented claims 27-30, respectively.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6-9, 11-13, 15-18, 20-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Nesheim et al. U.S. Patent 5,897,664.

As per claim 6, Nesheim teaches a host computing system, comprising: a processor; memory (column 6, lines 50-60); means for establishing a connection between the memory and memory of a target computer; a data retrieval component configured to transfer address data from memory of the target computer to the memory; an address translation component configured to replicate virtual memory addresses from the address data in the memory (column 7, lines 13-27; column 8, lines 33-43; column 10, lines 8-14).

As per claim 7, Nesheim teaches the host computing system as recited in claim 6, further comprising cache memory configured to store the replicated virtual memory addresses (column 4, lines 42-47).

Art Unit: 2113

As per claim 8, Nesheim teaches the host computing system as recited in claim 6, wherein the host-side address translation component is further configured to validate the replicated virtual memory addresses (column 7, lines 23-28).

As per claim 9, Nesheim teaches the host computing system as recited in claim 6, further comprising a memory management verifier that verifies that a processor of the target computing system has memory management enabled (column 7, lines 1-2).

As per claim 11, Nesheim teaches a method, comprising: accessing address tables from physical memory of a target computer system; replicating the address tables on a host computing system; and using data contained in the address tables to derive virtual address data that was used on the target computer system (column 5, lines 15-52; column 7, lines 10-27; column 8, lines 32-50; column 10, lines 8-14).

As per claim 12, Nesheim teaches the method as recited in claim 11, further comprising storing the address tables in memory on the host computer system (column 8, lines 49-52).

As per claim 13, Nesheim teaches the method as recited in claim 11, further comprising caching the virtual address data on the host computer system (column 4, lines 43-47).

As per claim 15, Nesheim teaches the method as recited in claim 11, further comprising determining if memory management of a target computer system processor is enabled (column 7, lines 1-2).

As per claim 16, Nesheim teaches the method as recited in claim 11, further comprising performing the method only if memory management of a target computer system processor is enabled (column 7, lines 1-2; wherein Neishem does not teach the MMU not enabled).

As per claim 17, Nesheim teaches the method as recited in claim 11, wherein the accessing further comprises: locating the address tables in physical memory of the target computer system; and reading the address tables from the target computer (column 5, lines 15-52).

As per claim 18, Nesheim teaches the method as recited in claim 11, further comprising validating the virtual address data to ensure it is identical to the virtual address data stored on the target computer system (column 7, lines 23-28).

As per claim 20, Nesheim teaches a computer-readable medium containing processor-executable instructions that, when executed on a processor, perform the method of claim 11 (column 5, lines 15-52; column 7, lines 10-27; column 8, lines 32-50; column 10, lines 8-14).

As per claim 21, Nesheim teaches one or more computer-readable media containing computer-executable instructions that, when executed by a computer, perform the following steps: transferring physical memory data contained of a target computer to a host computer; translating address data contained in the physical memory data to virtual addresses utilized by the target computer (column 7, lines 10-27; column 8, lines 32-50; column 10, lines 8-14).

As per claim 22, Nesheim teaches the one or more computer-readable media as recited in claim 21, further comprising computer-executable instructions that, when executed by a computer, perform the following steps: locating address data in the physical memory of the target computer; and transferring only the address data to the host computer (column 7, lines 23-27).

As per claim 23, Nesheim teaches the one or more computer-readable media as recited in claim 21, further comprising computer-executable instructions that, when executed by a

Art Unit: 2113

computer, caches data transferred from the target computer on the host computer (column 4, lines 42-47).

As per claim 24, Nesheim teaches the one or more computer-readable media as recited in claim 21, further comprising computer-executable instructions that, when executed by a computer, validating the transferred data to determine if the transferred data is identical to the contents of the physical memory (column 7, lines 18-27).

As per claim 25, Nesheim teaches the one or more computer-readable media as recited in claim 21, further comprising computer-executable instructions that, when executed by a computer, determining if memory management is enabled on a processor in the target computer prior to transferring data (column 7, lines 1-2; column 10, lines 8-14; column 9, lines 7-11).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-5, 10, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nesheim in view of Brandewie U.S. Patent 6,094,530.

As per claim 1, Nesheim teaches a method for a target computer that utilizes virtual memory paging for the method comprising: transferring physical memory data from the target computer to a host computer; and replicating virtual memory data from the physical memory

Art Unit: 2113

data on the host computer (column 7, lines 10-27; column 8, lines 32-50; column 10, lines 8-14). Nesheim does not explicitly teach of the debugging of the target system. Brandewie does teach the debugging of the target system (column 2, lines 31-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the debugging process of Brandewie in the process of Nesheim. One of ordinary skill in the art would have been motivated to use the debugging process of Brandewie in the process of Nesheim because Brandewie teaches the benefit of replicating data locally from a remote source wherein the remote data could be in non-contiguous regions of memory (column 3, lines 9-12) and still have up-to-date replication on the local host to ensure coherency (column 2, lines 63-65); this is an explicit desire of Nesheim in that coherency is important in the replication (column 7, lines 13-27) and non-contiguous ranges replication from the remote node are also desired in the virtual memory transfer system of Nesheim (column 10, lines 50-56).

As per claim 2, Nesheim teaches the method as recited in claim 1. Nesheim does not teach further comprising debugging a fault on the target computer by analyzing replicated data on the host computer. Brandewie does teach debugging a fault on the target computer by analyzing replicated data on the host computer (column 2, lines 31-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the debugging process of Brandewie in the process of Nesheim. One of ordinary skill in the art would have been motivated to use the debugging process of Brandewie in the process of Nesheim because Brandewie teaches the benefit of replicating data locally from a remote source wherein the remote data could be in non-contiguous regions of memory (column 3, lines 9-12) and still have up-to-date replication on the local host to ensure coherency (column 2, lines 63-



65); this is an explicit desire of Nesheim in that coherency is important in the replication (column 7, lines 13-27) and non-contiguous ranges replication from the remote node are also desired in the virtual memory transfer system of Nesheim (column 10, lines 50-56).

As per claim 3, Nesheim teaches the method as recited in claim 1, further comprising caching the replicated data in memory on the host computer (column 4, lines 42-47).

As per claim 4, Nesheim teaches the method as recited in claim 1, wherein the target computer includes an operating system that uses table-driven paged memory management (column 8, lines 47-52).

As per claim 5, Nesheim teaches the method as recited in claim 1, wherein: the target computer includes a processor that has halted execution; and the virtual memory data is located in physical memory of the target computer (column 7, lines 13-28; column 6, lines 61-67).

As per claim 10, Nesheim teaches the host computing system as recited in claim 6, wherein the means for establishing a connection between the memory and memory of a target computer (column 6, lines 51-53). Nesheim does not teach wherein the connection comprises hardware-assisted debug probes. Brandewie does teach wherein the connection comprises hardware-assisted debug probes (column 2, lines 17-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the debugging process of Brandewie in the process of Nesheim. One of ordinary skill in the art would have been motivated to use the debugging process of Brandewie in the process of Nesheim because Brandewie teaches the benefit of replicating data locally from a remote source wherein the remote data could be in non-contiguous regions of memory (column 3, lines 9-12) and still have up-to-date replication on the local host to ensure coherency (column 2, lines 63-65); this is an

Art Unit: 2113

explicit desire of Nesheim in that coherency is important in the replication (column 7, lines 13-27) and non-contiguous ranges replication from the remote node are also desired in the virtual memory transfer system of Nesheim (column 10, lines 50-56).

As per claim 19, Nesheim teaches the method as recited in claim 11, further comprising analyzing the virtual address data on the host computer system (column 7, lines 10-27; column 8, lines 32-50; column 10, lines 8-14). Nesheim does not teach debugging a fault that occurred on the target computer by analyzing the data on the host computer system. Brandewie does teach debugging a fault that occurred on the target computer by analyzing the data on the host computer system (column 2, lines 31-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the debugging process of Brandewie in the process of Nesheim. One of ordinary skill in the art would have been motivated to use the debugging process of Brandewie in the process of Nesheim because Brandewie teaches the benefit of replicating data locally from a remote source wherein the remote data could be in non-contiguous regions of memory (column 3, lines 9-12) and still have up-to-date replication on the local host to ensure coherency (column 2, lines 63-65); this is an explicit desire of Nesheim in that coherency is important in the replication (column 7, lines 13-27) and non-contiguous ranges replication from the remote node are also desired in the virtual memory transfer system of Nesheim (column 10, lines 50-56).

***Allowable Subject Matter***

Art Unit: 2113

7. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/826,228

Page 11

Art Unit: 2113

January 11, 2006

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